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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,483	05/24/2005	Bruce B Doris	FIS920020105	6798
32074	7590	06/29/2007		
INTERNATIONAL BUSINESS MACHINES CORPORATION DEPT. 18G BLDG. 300-482 2070 ROUTE 52 HOPEWELL JUNCTION, NY 12533			EXAMINER LIU, BENJAMIN T	
			ART UNIT	PAPER NUMBER
			2826	
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			06/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/536,483

Applicant(s)

DORIS ET AL.

Examiner

Benjamin T. Liu

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 February 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

1. Claims 9-17 canceled in amendment submitted 2/20/07.

Response to Arguments

2. Applicant's arguments filed 2/20/07 have been fully considered but they are not persuasive.

Regarding claim 1, applicant argues on page 4 of the arguments that Lin nor Ito teaches the PMOS or NMOS devices having a compressive layer that induces compressive or tensile stress in the active region "in a direction longitudinal to a current direction". However, figures 4 and 9 and par [0025], [0027] of Lin et al. discloses "capping layer 920 remains after fin 910 is etched so that fin 910 is strained to improve mobility". The stress that the capping layer 920 induces on the fin 910 is not restricted to only the direction latitudinal to the current direction. The capping layer 920 would induce stress on the fin 910 in both longitudinal and latitudinal direction thus reading on claim 1. Claim 1 rejected.

Claim Rejections - 35 USC § 102(e)

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5, and 7-8 are rejected under 35 U.S.C 102(e) as being anticipated by Lin et al. (2004/0075122).

With regard to claim 1, figures 4 and 9 of Lin et al. disclose a semiconductor device structure, comprising: a FinFET that provides CMOS compatibility, which are a PMOS device and an NMOS device disposed on a substrate 200, the cover layer 920 providing a tensile strain good for electron mobility or compressive stress good for hole mobility, which inherently disclose the PMOS device including a compressive layer (920 of PMOS) inducing a compressive stress in an active region of the PMOS device in a direction longitudinal to a current direction, the NMOS device including a tensile layer (920 of NMOS) inducing a tensile stress in an active region of the NMOS device in a direction longitudinal to the current direction, wherein the compressive layer (920 of PMOS) includes a first dielectric material (920 of PMOS), the tensile layer (920 of NMOS) includes a second dielectric material (920 of NMOS), and the PMOS and NMOS devices are FinFET devices 400. (Note lines 11-12 in paragraph [0003] and paragraphs [0025] and [0027] of Lin et al.)

Regarding claim 1, applicant argues on page 4 of the arguments that Lin nor Ito teaches the PMOS or NMOS devices having a compressive layer that induces compressive or tensile stress in the active region "in a direction longitudinal to a current direction". However, figures 4 and 9 and par [0025], [0027] of Lin et al. discloses "capping layer 920 remains after fin 910 is etched so that fin 910 is strained to improve mobility". The stress that the capping layer 920 induces on the fin 910 is not restricted to only the direction latitudinal to the current direction. The capping layer 920 would

induce stress on the fin 910 in both longitudinal and latitudinal direction thus reading on claim 1. Claim 1 rejected.

With regard to claim 2, figures 4 and 9 of Lin et al. disclose a semiconductor device, wherein the first dielectric material (920 of PMOS) comprises SiN. (Note lines 11-12 in paragraph [0003], lines 19-20 in paragraph [0020], and paragraphs [0025] and [0027] of Lin et al.)

With regard to claim 3, figures 4 and 9 of Lin et al. disclose a semiconductor device, wherein the second dielectric material (920 of NMOS) comprises SiN. (Note lines 11-12 in paragraph [0003], lines 19-20 in paragraph [0020], and paragraphs [0025] and [0027] of Lin et al.)

With regard to claim 5, figures 4 and 9 of Lin et al. disclose semiconductor device structure, wherein the first dielectric material (920 of PMOS) has a substantially uniform thickness in a range of 200A to 2000A. (Note paragraph [0027] of Lin et al.)

With regard to claim 7, figures 4 and 9 of Lin et al. disclose a semiconductor device structure, wherein the second dielectric material (920 of NMOS) has a substantially uniform thickness in a range of 200A to 2000A. (Note paragraph [0027] of Lin et al.)

With regard to claim 8, figures 4 and 9 of Lin et al. disclose a semiconductor device structure, wherein the first dielectric material (920 of PMOS) and the second dielectric material (920 of NMOS) are SiN. (Note lines 11-12 in paragraph [0003] and paragraphs [0025] and [0027] of Lin et al.)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4 and 6 are rejected under 35 U.S.C 103(a) as being unpatentable over Lin et al. (2004/0075122) in view of Ito (2002/0081794).

With regard to claim 4, Lin et al. discloses all the subject matter claimed except for the first dielectric material having a substantially uniform compressive stress in a range of -300 MPa to -3000 MPa.

However, figures 2C and 5 of Ito do disclose the first dielectric material (9 of PMOS) having a substantially uniform compressive stress in a range of -300 MPa to -3000 MPa.

Therefore, it would have been obvious to one of ordinary skill in the art to form the semiconductor device of Lin et al. with the dielectric material of Ito in order to increase the hole mobility of the transistor.

With regard to claim 6, Lin et al. discloses all the subject matter claimed except for the second dielectric material having a substantially uniform tensile stress in a range of +200 MPa to +2000 MPa.

However, figures 2C and 5 of Ito do disclose the second dielectric material (9 of NMOS) having a substantially uniform tensile stress in a range of +200 MPa to +2000 MPa.

Therefore, it would have been obvious to one of ordinary skill in the art to form the semiconductor device of Lin et al. with the dielectric material of Ito in order to increase the electron mobility of the transistor.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin T. Liu whose telephone number is (571) 272-6009. The examiner can normally be reached on Mon-Fri 9:30 AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on 571 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BTL
6/23/2007


SUE A PURVIS
SUPERVISORY PATENT EXAMINER